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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,289	06/15/2001	Helmut Wurzer	12816-018001 / S1187 SB	6868

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EXAMINER
GOUDREAU, GEORGE A

ART UNIT	PAPER NUMBER
1763	

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-882,289	Wurzer et al.
Examiner	**Group Art Unit**
George Goldrean	1763

—The MAILING DATE of this communication appears on th cover sheet beneath th correspondence address—

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 (MONTH(S)) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 6-03 (Re - paper #15)

☒ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 8-19 is/are pending in the application.

Of the above claim(s) 16-19 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 8, 10-15 is/are rejected.

☒ Claim(s) 9 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. § 119 (a)-(d)

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☒ All ☐ Some* ☐ None of the:

☒ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 9

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Int rvi w Summary, PTO-413

☐ Notice of Informal Pat nt Applicati n, PTO-152

☐ Oth r _____

Office Action Summary

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Kawasaki et. al. (JP 51-145,267).

Kawasaki et. al. disclose a process for forming a device which is comprised of the following steps:

-A first silicon layer is formed on the front side of a sapphire substrate.;

-A SiO2 layer is formed onto the first silicon layer on the front side of the wafer.;

-N ions are implanted through the SiO2 layer on the front side of the wafer such that they form a Si3N4 layer at the interface of the SiO2 layer with the underlying Si layer.; and

-The SiO2 layer on the front side of the wafer is then removed.

This is discussed specifically in the abstract, and discussed in general on pages 369-371. This is shown in figures 1-7.

3. Claims 8, 10, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki et. al. (JP 05-283,679).

Kusunoki et. al. disclose a process for forming a device which is comprised of the following steps:

-Source/drain regions (104, 105) are formed onto the front face of a Si wafer (101).;

-A SiO2 pad oxide layer (102) is grown onto the surface of the Si wafer.;

-The SiO2 pad oxide layer is thermally treated with either NO gas or NH3 gas to form a SiON layer at the interface of the SiO2 layer with the Si substrate.;

-A N-doped metal gate layer is formed onto the surface of the pad layer (102).; and

-The N-doped metal gate layer, the SiO2 pad layer (107), and the SiON pad layer (106) are then etched.

This is discussed specifically in the abstract; and discussed in general on pages 1-9. This is shown in figures 1-7.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 10-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et. al. (JP 51-145,267) as applied in paragraph 2 above.

Kawasaki et. al. (JP 51-145,267) as applied in paragraph 2 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a thermal annealing in a N2 based atmosphere such as any of N2, N2O, or NO plus NH3 to form the Si3N4 layer at the interface of the SiO2 layer, and the Si layer in the process taught above; and

-the specific usage of either a dry or a wet etching process to etch the SiO2 layer in the process taught above

It would have been obvious to one skilled in the art to replace the N2 ion implant step used to form the Si3N4 layer at the interface of the SiO2 layer, and the Si layer in the process taught above with a thermal annealing step in an atmosphere of any of N2, N2O, or NO plus NH3 based upon the following. The specific usage of a thermal annealing step in an atmosphere of any of N2, N2O, or NO plus NH3 to form a Si3N4 layer on the surface of a SiO2 layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming a Si3N4 layer in the process taught above to the specific means which are taught above.

It would have been obvious to one skilled in the art to use either a dry or wet etching process to remove the SiO2 layer from the underlying Si3N4 layer in the process taught above based upon the following. The usage of either a dry or wet etching process to remove a SiO2 layer from an underlying Si3N4 layer on a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for etching the SiO2 layer in the process taught above to the specific means which are taught above.

7. Claims 11, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et. al. (JP 05-283,679) as applied in paragraph 3 above.

Kusunoki et. al. (JP 05-283,679) as applied in paragraph 3 above fail to disclose the following aspects of applicant's claimed invention:

-the specific usage of a thermal annealing in a N2 based atmosphere such as any of N2, N2O, or NO plus NH3 to form the SiON layer at the interface of the SiO2 layer, and the Si layer in the process taught above; and

-the specific usage of either a wet or dry etching process to etch the SiO2 layer in the process taught above

It would have been obvious to one skilled in the art to replace the NO or NH3 thermal annealing step used to form the SiON layer at the interface of the SiO2 layer, and the Si layer in the process taught above with a thermal annealing step in an atmosphere of any of N2, N2O, or NO plus NH3 based upon the following. The specific usage of a thermal annealing step in an atmosphere of any of N2, N2O, or NO plus NH3 to form a SiON layer on the surface of a SiO2 layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming a SiON layer in the process taught above to the specific means which are taught above. Also, this reference teaches that it was known in the prior art to employ a thermal annealing step in an N2O atmosphere to form a SiON layer at the interface of a SiO2 layer with a Si layer.

It would have been obvious to one skilled in the art to use either a dry or wet etching process to remove the SiO2 layer from the underlying SiON layer in the process taught above based upon the following. The usage of either a dry or wet etching process to remove a SiO2 layer from an underlying SiON layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for etching the SiO2 layer in the process taught above to the specific means which are taught above.

8. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag
Primary Examiner
AU 1763